Appl. No. 10/076,977

Amdt. Dated January 14, 2004

Reply to Office Action of October 15, 2003

SPECIFICATION AMENDMENTS

The paragraph beginning at line 18 on page 3 is revised as follows:

It is accordingly an object of the invention to provide a test system for conducting a function test of a semiconductor element on a wafer, and operating method that overcomes the hereinafore mentioned aforementioned disadvantages of the heretofore-known devices and methods of this general type and that increases the precision with which a supply voltage can be applied to corresponding terminal pads of the element being tested.

The paragraph beginning at line 1 on page 5 is revised as follows:

The invention is, thus, based on the idea of extending a read line through a read contact pin to a terminal pad of the module being tested. By regulating the output voltage delivered by the voltage source base based upon the electrical potential of the read contact pin, it is possible to adjust the supply voltage to the desired value notwithstanding a transitional resistance between the supply contact pin and the terminal pad.

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The paragraph beginning at line 25 on page 6 is revised as follows:

The current drawn by the modules also remains approximately constant given a dropping supply voltage Vcc, so that the voltage drop due to a transitional resistance between the supply pins and the terminal pad remains approximately the same. However, due to the dropping absolute value of the supply voltage, the error percentage generated by the voltage drop increases from generation to generation accordingly.

The paragraph beginning at line 1 on page 12 is revised as follows:

The supply voltage is provided by the programmable voltage source 12 and conducted to the corresponding terminal pads 44, 46 by way of current drive lines 14, 16. The lines 14, 16 lead to a pin card configuration 20, which includes a test head 22, ZIF connector 24, motherboard 26, pogo pins 28, and a pin card board 30. The individual elements of the pin card configuration 20 are represented in FIG. 1 only schematically.